IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use in a network interface controller, a power source and power management signaling control system comprising:

a voltage regulator;

a first connection coupled to the voltage regulator for connection to a network-initiated power management recovery signal and a power management recovery bus signal; [[and]]

a second connection coupled to the voltage regulator for selective connection to a motherboard header; and [[,]]

an inverter capable of gating auxiliary power for a network interface card to main power for the network interface card when a bus power signal is asserted and disconnecting the auxiliary power from the main power when the bus power signal is not asserted;

wherein the control system is operable to provide power to [[a]] the network interface card and power management signals, if necessary, within each of: a system [[s]] not supporting network-initiated power management recovery, a system [[s]] supporting network-initiated power management recovery through the header, and a system [[s]] supporting network-initiated power management recovery through the power management recovery bus signal.

2. (Currently Amended) The control system according to claim 1, further comprising:

a third connection coupled to the voltage regulator for connection to an auxiliary power bus signal; [[,]]

wherein the control system is operable to provide the auxiliary power to the network interface card within a system [[s]] not providing auxiliary power, within a system [[s]] providing auxiliary power from the header, and within a system [[s]] providing auxiliary power from the auxiliary power bus signal.

3. (Original) The control system according to claim 2, wherein grounding of the auxiliary power bus signal does not affect provision of auxiliary power to the network interface card by the control system.

4. (Currently Amended) The control system according to claim 1, further comprising:

[[an]] a second inverter inverting the network-initiated power management recovery signal to the header.

5. (Cancelled).

6. (Original) The control system according to claim 1, further comprising:

diodes preventing back powering of a bus to which the control system is coupled during hibernate states, system power short circuiting of and leakage malfunctions in the control system when the header is incorrectly connected or unconnected to the motherboard, and auxiliary power shorts to ground when an auxiliary power bus signal coupled to the control system is grounded.

7. (Currently Amended) The control system according to claim 1, wherein the control system is operable within a system [[s]] that does not provide 3.3V power to provide 3.3V power from the voltage regulator.

8. (Currently Amended) A network interface controller comprising:

connections for selectively coupling the controller to a network interface card adapted for installation within a Peripheral Component Interconnect (PCI) bus slot; and

a power control circuit coupled to the connections, the control circuit comprising:

a first connection coupling a voltage regulator to a network-initiated power management recovery signal and a power management recovery bus signal; and

a second connection selectively coupling the voltage regulator to a motherboard header; and [[,]]

diodes capable of preventing back powering of a bus to which the control circuit is coupled during hibernate states, system power short circuiting of and leakage malfunctions in the control circuit when the header is incorrectly connected or unconnected to the motherboard, and auxiliary power shorts to ground when an auxiliary power bus signal coupled to the control circuit is grounded;

wherein the controller is operable to provide power to the network interface card within any of: a system [[s]] not supporting network-initiated power management recovery, a system [[s]] supporting network-initiated power management recovery through the header, and a system [[s]] supporting network-initiated power management recovery through the power management recovery bus signal.

9. (Currently Amended) The controller according to claim 8, further comprising:

a third connection coupling the voltage regulator to [[an]] the auxiliary power bus signal; [[,]]

wherein the control circuit is operable to provide auxiliary power to the network interface card within a system [[s]] not providing auxiliary power, within a system [[s]] providing auxiliary power from the header, and within a system [[s]] providing auxiliary power from the auxiliary power bus signal.

10. (Original) The controller according to claim 9, wherein grounding of the auxiliary power bus signal does not affect provision of auxiliary power to the network interface card by the control circuit.

11. (Original) The controller according to claim 8, further comprising:

an inverter inverting the network-initiated power management recovery signal to the header.

12. (Original) The controller according to claim 8, further comprising:

an inverter gating auxiliary power for the network interface card to main power for the network interface card when a bus power signal is asserted and disconnecting the auxiliary power from the main power when the bus power signal is not asserted.

13. (Cancelled).

14. (Currently Amended) The controller according to claim 8, wherein the control circuit is operable within a system [[s]] that does not provide 3.3V power to provide 3.3V power from the voltage regulator.

15. (Currently Amended) For use in a network interface controller, a method of power and power management signaling control comprising:

providing a single voltage regulator coupled to a network-initiated power management recovery signal and a power management recovery bus signal, [[and]] selectively coupled to a motherboard header, and coupled to an auxiliary power bus signal if available; [[and]]

operating a control system for the voltage regulator to provide power to a network interface card and power management signals, if necessary, independent of whether the controller is installed within a system not supporting network-initiated power management recovery, a system supporting network-initiated power management recovery through the header, or a system supporting network-initiated power management recovery through the power management recovery bus signal;

operating the control system to provide auxiliary power to the network interface card independent of whether the controller is installed within a system not providing auxiliary power, a system providing auxiliary power from the header, or a system providing auxiliary power from the auxiliary power bus signal; and

providing auxiliary power to the network interface card independent of whether the auxiliary power bus signal is grounded.

16. (Cancelled).

17. (Cancelled).

18. (Original) The method according to claim 15, further comprising:

inverting the network-initiated power management recovery signal to the header.

19. (Original) The method according to claim 15, further comprising:

gating auxiliary power for the network interface card to main power for the network interface card when a bus power signal is asserted; and

disconnecting the auxiliary power from the main power when the bus power signal is not asserted.

20. (Original) The method according to claim 15, further comprising:

preventing back powering of a bus to which the control system is coupled during hibernate states;

preventing system power short circuiting of and leakage malfunctions in the control system when the header is incorrectly connected or unconnected to the motherboard; and

preventing auxiliary power shorts to ground when an auxiliary power bus signal coupled to the control system is grounded.

21. (New) The control system according to claim 4, wherein the second inverter is capable of inverting the network-initiated power management recovery signal to generate a Power Management Event (PME) signal for the motherboard header.

22. (New) The control system according to claim 1, wherein the inverter comprises:

a first transistor coupled to the main power and the auxiliary power; and

a second transistor coupled to the first transistor, the auxiliary power, and the bus power signal.

23. (New) The network interface controller according to claim 12, wherein the inverter comprises:

a first transistor coupled to the main power and the auxiliary power; and

a second transistor coupled to the first transistor, the auxiliary power, and the bus power signal.

24. (New) The method according to claim 18, wherein inverting the network-initiated power management recovery signal comprises inverting the network-initiated power management recovery signal to generate a Power Management Event (PME) signal for the motherboard header.